Current-Mode Class-D Power Amplifiers for High-Efficiency RF Applications

Hidenori Kobayashi, *Member, IEEE*, Jeffrey M. Hinrichs, and Peter M. Asbeck, *Fellow, IEEE*

***Abstract*—We show that current-mode class-D (CMCD) power amplifiers can achieve high efficiency at RF frequencies. In contrast with conventional voltage-mode class-D amplifiers, the CMCD features "zero voltage switching," which eliminates the output capacitance discharge loss. Experimental CMCD amplifiers with 76.3% power-added efficiency (PAE) at 290-mW output and 71.3% PAE at 870-mW output are demonstrated using GaAs FETs at 900 MHz.**

***Index Terms*—Analog circuits, MESFET power amplifiers, power amplifiers, wireless communications.**

I. Introduction

SWITCHING-MODE power amplifiers have the potential for high efficiency, with drain efficiency theoretically approaching 100% [1]. However, available transistors are not ideal switches because of parasitic reactances, finite on-resistance, and limited gain. Class-D amplifiers are popular switching-mode amplifiers for audio frequencies. However, they exhibit poor efficiency at higher frequencies because parasitic reactances lead to substantial loss [2]. If transistor switches have output shunt capacitance C (and not too large series inductance), then energy $1/2CV^2$ is dissipated each cycle, where V is the voltage across the transistor at switch closure. The class-E approach can solve these problems [3]. When the transistors turn on and the switches close, the voltage across the devices is always zero so output capacitance discharge loss is avoided [i.e., zero-voltage-switching (ZVS)]. This approach works well up to the megahertz frequency range, but is less effective in the gigahertz range. Uncertain duty cycle due to sinusoidal driving waveforms, nonlinear capacitances, and other parasitic components degrade the class-E operation. Multiharmonic load termination [4], class-F [5], and inverse class-F (tuned class B) [6], [7] are other less well-developed techniques to achieve ZVS (or zero-current-switching (ZCS), a related condition that minimize series inductances losses). Here, we describe another approach that can achieve ZVS, the current-mode class-D (CMCD) amplifier. This is related to the more frequently used voltage-mode class-D amplifier by an interchange between voltage and current waveforms. In this paper, the CMCD is demonstrated with GaAs FETs to achieve $>$75% power-added efficiency (PAE) at 900 MHz.

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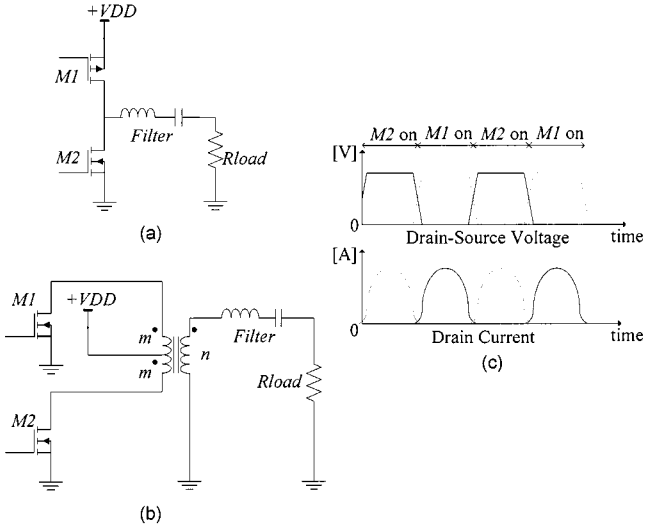


Fig. 1. VMCD circuits and waveforms. (a) VMCD circuit 1. (b) VMCD circuit 2. (c) Current and voltage waveform.

II. Concept of CMCD

Fig. 1 shows the basic schematic of a voltage mode class-D (VMCD) amplifier (sometimes referred to only as "class-D"). The fundamental circuit and a more practical realization are shown in Fig 1(a) and Fig 1(b), respectively. Two transistors are driven 180° out-of-phase. A series filter is employed, with a resonant frequency set to the center frequency of the signal. Ideal drain voltage and drain current waveforms are shown in Fig 1(c). The voltage across the transistors is a square wave and the transistor current becomes a half-wave rectified sine wave. However, if the transistors have some output capacitance $C_{\rm DS}$, this capacitance must be charged or discharged to $V_{\rm DD}$ or ground through the transistor. That means that the voltage waveform cannot have a perfect square shape and some transient current spikes occur when the transistor turns on. The overlapping of voltage and current cannot be avoided. This loss can be described by an energy loss E_c per cycle with E_c given by

$$E_c = \frac{1}{2} C_{\rm DS} \cdot V_{\rm DS-OFF}^2 \tag{1}$$

where $C_{\rm DS}$ is the drain–source capacitance and $V_{\rm DS-OFF}$ is the drain–source voltage when the transistor is turned on. This output capacitance loss is independent of the channel resistance of the transistor and becomes the dominant loss mechanism at

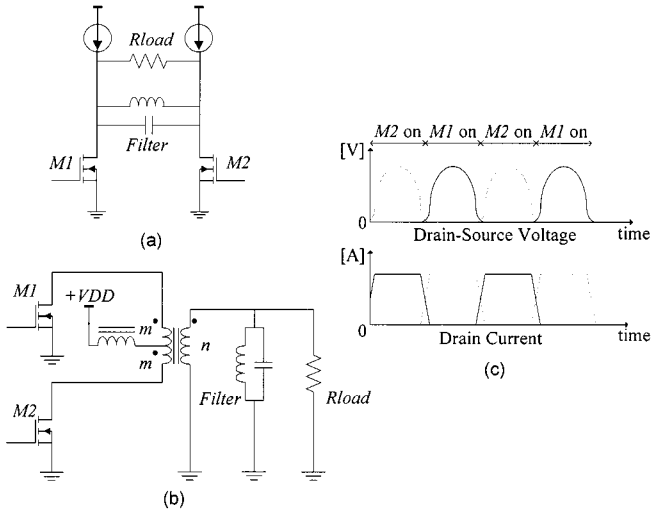


Fig. 2. CMCD circuits and waveforms. (a) CMCD circuit 1. (b) CMCD circuit 2. (c) Current and voltage waveform.

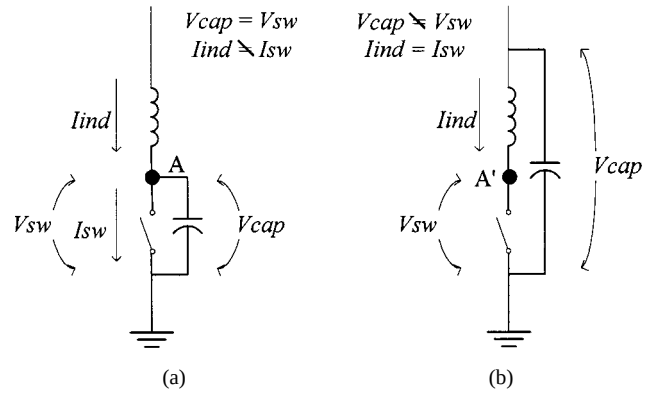


Fig. 3. Switch models.

high frequencies starting at hundreds of megahertz. This is one of the reasons that class-D is not a popular gigahertz amplifier. Fig. 2(a) and (b) shows the CMCD circuits and Fig. 2(c) shows the waveforms for each transistor. For the CMCD, we use current sources instead of voltage sources, and the two switching transistors control the current instead of the voltage. There is a parallel-connected filter, with resonant frequency set to the carrier frequency. Due to the filter resonance, there is no voltage across the transistors at each switching time and so-called ZVS is achieved. Even if the transistors have some output capacitance, the output capacitance can become part of the output parallel filter; voltage waveforms are still as shown in Fig. 2(c). This ZVS feature is a key advantage of the CMCD architecture.

As mentioned above, another important switching condition, i.e., ZCS, avoids inductance losses by making the current zero at the instant of switching. VMCD and class-F achieve this condition. However, ZCS is less important than ZVS. Fig. 3(a) and (b) shows examples of switches with parasitic inductance and capacitance in different topologies. In Fig. 3(a), the capacitance voltage and the switch voltage are identical. Thus, if there is voltage when the switches turn on, $1/2CV^2$ energy is lost, and ZVS is needed at node A to avoid this loss. However, current can continue to flow to the capacitor when switches turn off and the inductance loss is eliminated. On the contrary, the capacitance loss is eliminated and inductance loss $1/2LI^2$ is unavoidable without ZCS at node A in Fig. 3(b). In practice, transistors are modeled more accurately as Fig. 3(a) than Fig. 3(b). Additionally, in suitable integrated-circuit (IC) implementation, the drain inductance can be minimized.

Another advantage of the CMCD amplifier is ease of implementation at high frequency. The VMCD amplifier typically requires complementary devices or a center-tapped transformer to function properly. The CMCD amplifier only requires a simple balun structure.

III. Theoretical Analysis of CMCD

In an ideal situation, the drain–source voltage $V_{\rm DS1}$, $V_{\rm DS2}$ are half-rectified sine waves and the drain currents $I_{\rm ds1}$, $I_{\rm ds2}$ are square waves. The current sources are ideal chokes tied to voltage source $V_{\rm DD}$, as shown in Fig. 2(b). The peak drain voltage can be calculated by

$$\int_0^T V_{\rm DS}(t)\cdot dt = \int_0^{T/2} V_{\rm peak}\cdot \sin(\omega t)\cdot dt = T\cdot Vdd \tag{2a}$$

$$V_{\rm peak} = \pi \cdot Vdd. \tag{2b}$$

Let us suppose the transformer ratio $n:m$ is $2:1$ in Fig. 2(b). Power output can be calculated by

$$P_{\rm OUT} = \frac{1}{2}\frac{(\pi\cdot V_{\rm DD})^2}{R_{\rm load}}. \tag{3}$$

In an ideal situation, $P_{\rm OUT}$ and $P_{\rm IN}$ are the same, thus, the dc drain current can be expressed as

$$I_{\rm DC} = P_{\rm OUT}/V_{\rm DD}. \tag{4}$$

However, (2a)–(4) are too ideal to properly represent real RF amplifiers. High-order harmonic frequencies are needed for perfect half-rectified sine or square waves. In RF frequency operation, it is very difficult to control impedance for the high-order harmonics due to the frequency dependence of each component. A more realistic estimate results from ignoring harmonic components of $V_{\rm DS}$ and $I_{\rm DS}$ greater than third order. The parallel filter and balanced circuits are still considered ideal in this calculation. In this case, the load line appears open to second harmonics and short to third harmonics. The voltage and current can be described as

$$V_{\rm DS}(t) = V_{\rm DD} + V_1\sin(\omega t) - V_2\cos(2\omega t) \tag{5a}$$

$$I_{\rm DS}(t) = I_{\rm DC} - I_1\sin(\omega t) - I_3\sin(3\omega t). \tag{5b}$$

We suppose the transistors' drain voltage and current never becomes negative. This can be expressed by

$$\begin{cases} \min.\{V_{\rm DS}(t)\} = 0 \\ \min.\{I_{\rm DS}(t)\} = 0. \end{cases} \tag{6}$$

To represent the switching operation, we consider V_2 and I_3 with the restriction that the waveform must be monotonically increasing during one half cycle and monotonically decreasing

during the other half cycle. The coefficients that achieve the above condition can be calculated from

$$\left.\frac{d^2V_{\rm DS}}{d^2t}\right|_{wt=(3/2)\pi}=0 \tag{7a}$$

$$\left.\frac{d^2I_{\rm DS}}{d^2t}\right|_{wt=(1/2)\pi,\,(3/2)\pi}=0. \tag{7b}$$

From (5)(7b), V_1, V_2, I_1, and I_3 can be determined to be

$$V_1=\frac{4}{3}V_{\rm DD} \tag{8a}$$

$$V_2=\frac{1}{3}V_{\rm DD} \tag{8b}$$

$$I_1=\frac{9}{8}I_{\rm DC} \tag{8c}$$

$$I_3=\frac{1}{8}I_{\rm DC}. \tag{8d}$$

If V_2 or I_3 are increased from these values, the waveforms develop multiple peaks and valleys.

Suppose the transformer ratio $n:m$ is $2:1$ in Fig. 2(b). The relationship of fundamental current and voltage can be expressed as

$$I_1=\frac{2\cdot V_1}{R_{\rm load}}. \tag{9}$$

Total dc input current, dc input power, and output power are given by

$$I_{\rm DC-total}=2\cdot I_{\rm DC}=\frac{16}{9}I_1 \tag{10a}$$

$$P_{\rm IN}=I_{\rm DC-total}\cdot V_{\rm DD} \tag{10b}$$

$$P_{\rm OUT}=\frac{1}{2}\frac{(2\cdot V_1)^2}{R_{\rm load}}=\frac{1}{2}\frac{(8/3\cdot V_{\rm DD})^2}{R_{\rm load}}. \tag{10c}$$

Transistors (switches) are not ideal in this case. There are simultaneous drain currents and voltages causing the transistors to dissipate energy $P_{\rm OUT}-P_{\rm IN}$. Waveforms of voltage and current are shown in Fig. 4. Table I shows corresponding values, along with efficiency for the case $V_{\rm DD}=3\,{\rm V}$ and $R_{\rm load}=50\,\Omega$.

Further analysis, including higher harmonics up to fifth harmonics, can be considered using (11a) and (11b), which are derived by similar considerations as follows:

$$V_{\rm DS}=V_{\rm DD}+\frac{64}{45}V_{\rm DD}\sin(\omega t)-\frac{4}{9}V_{\rm DD}\cos(2\omega t)-\frac{1}{45}V_{\rm DD}\cos(4\varpi t) \tag{11a}$$

$$I_{\rm DS}=I_{\rm DC}-\frac{75}{64}I_{\rm DC}\sin(\omega t)-\frac{25}{128}I_{\rm DC}\sin(3\omega t)-\frac{3}{128}I_{\rm DC}\sin(5\omega t). \tag{11b}$$

Results for this case are also shown in Fig. 4 and Table I. As we expect, efficiency increases if appropriate higher order harmonic terminations are used. Also, we can see that output power is very sensitive to harmonics terminations even when the fundamental load is fixed. On the contrary, dc input current (dc input power) is almost constant.

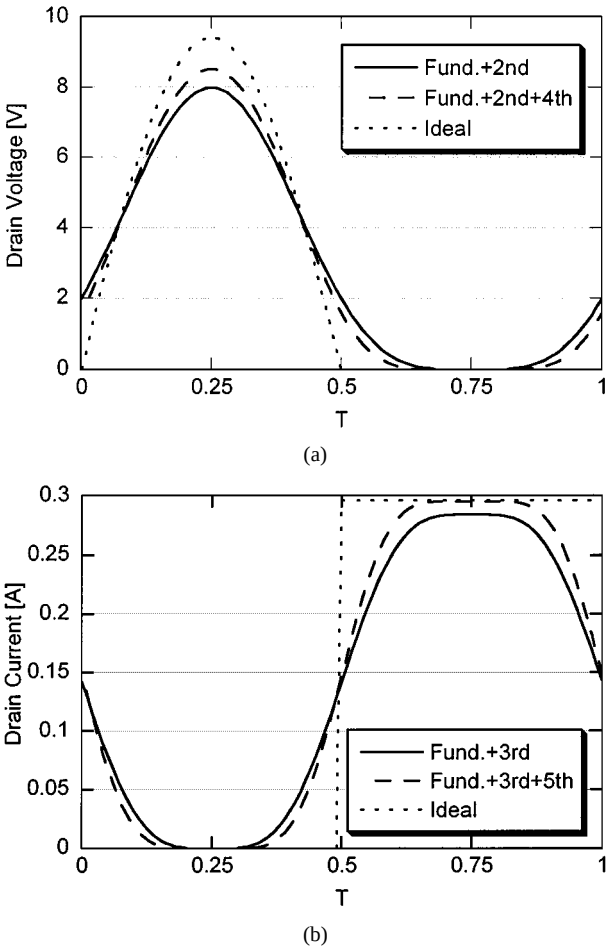


Fig. 4. CMCD analytical voltage and current waveforms. (a) Voltage waveforms. (b) Current waveforms ($V_{\rm DD}=3$ V, $R_{\rm load}=50\,\Omega$).

IV. PA Design and Simulation

The CMCD amplifier was implemented at 900 MHz with commercially available GaAs MESFETs (Infineon CLY5). Harmonic-balance simulations were performed with HP ADS. Statz MESFET model parameters of the chip transistor and the SOT223 package model were used. The CMCD circuits are redesigned using a 50-Ω coaxial balun and are shown in Fig. 5 (minor package parasitic components are omitted in this figure). Due to practical board layout constraints, 25-Ω transmission lines T_1 and T_2 are inserted between components. We optimized the lengths of T_1 and T_2, and the values of $C_{\rm ext}$ and $C_{\rm fil}$ to achieve ZVS at node A (not at the drain terminal of the transistor package) by simulation. Fig. 6 shows simulated voltage and current waveforms. Solid lines indicate chip drain–source voltage and current, and dotted lines are voltage and current including package parasitic components (mainly $L_{\rm D}$ and $C_{\rm DS}$). Due to device parasitic drain–source capacitance, the drain current does not look like a square wave, but becomes negative when the transistor is off. If we extract all output capacitances (including device capacitances), the current waveform should be more rectangular. In this simulation, we achieved 84% PAE at 25.4 dBm (0.35 W) with $V_{\rm DD}=3$ V.

TABLE I
THEORETICAL EFFICIENCY ($V_{\rm DD} = 3$ V AND $R_{\rm load} = 50\,\Omega$)

Maximum Harmonics	Drain Peak Voltage [V]	Total DC Current [mA]	Output Power [mW]	DC input power [mW]	Switch loss [mW]	Drain efficiency [%]
3rd	8	284	642	852	210	75.3%
5th	8.54	295	729	885	156	82.4%
All (∞)	9.42	296	887	887	0	100%

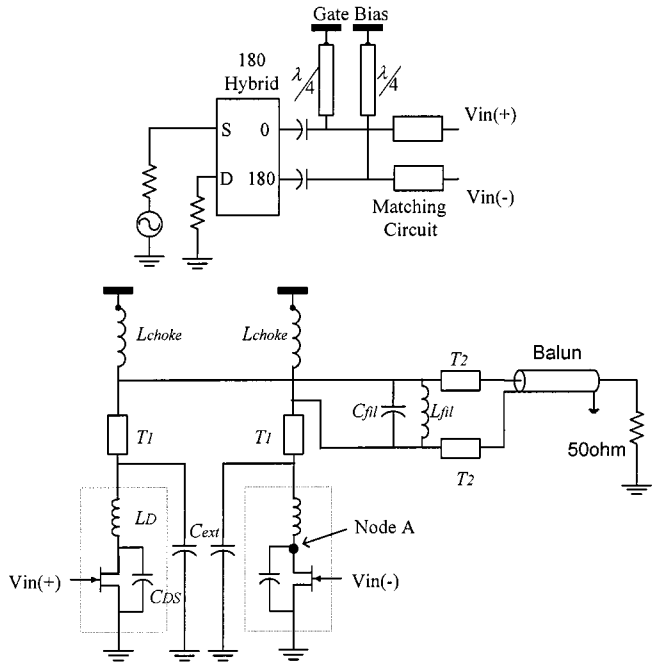


Fig. 5. CMCD circuits for high frequency.

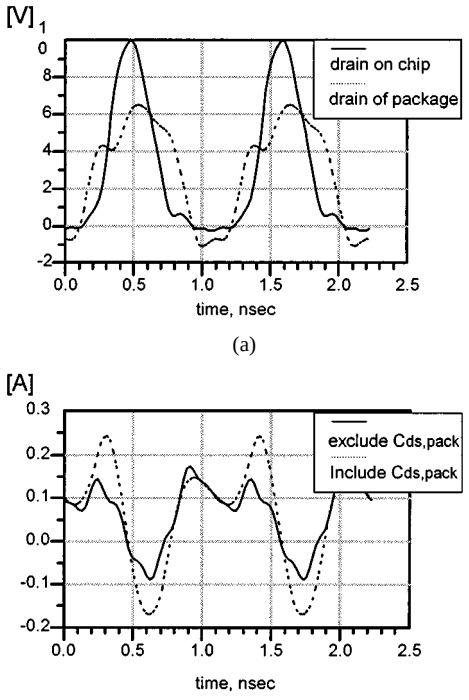


Fig. 6. Simulated voltage and current waveforms. (a) Voltage waveform. (b) Current waveform (operational frequency = 900 MHz).

V. EXPERIMENTAL RESULTS

A picture of the CMCD power amplifier is shown in Fig. 7. A Mini-Circuits 180° hybrid is used to generate the balanced signal for the input and input impedance-matching circuits are tuned for maximum gain. $C_{\rm ext}$ and $C_{\rm fil}$ in Fig. 5 are optimized for higher efficiency.

Fig. 8 shows the efficiency and RF output power when the gate-bias voltage is -1.7 V and $V_{\rm DD}$ is 3 V. The input power does not include the 180°-hybrid loss, but the output power includes output balun loss. The drain efficiency reaches 80% when the input power is above 11 dBm. The PAE reaches a peak value of 76.3% under these conditions. The corresponding power gain is approximately 12 dB. The gain decreases with increasing input power since the output power is nearly constant (and determined only by the power supply voltage). Fig. 9 shows the output power and efficiency when $V_{\rm DD}$ is 5 V. Drain efficiency of 75.6% and PAE of 72.5% was achieved with the input power set to 14.7 dBm and output set to 28.6 dBm (0.73 W). In both cases, output power is much smaller than the theoretical value we expected. One of the reasons is that we can only achieve up to third harmonic terminations, and even second and third harmonic terminations are not perfect because of device parasitic components. We believe that the nonideal RF choke especially decreases output power.

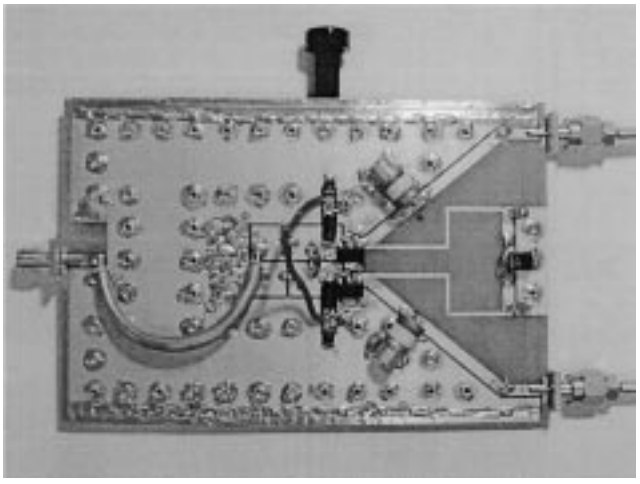


Fig. 7. CMCD PA circuit.

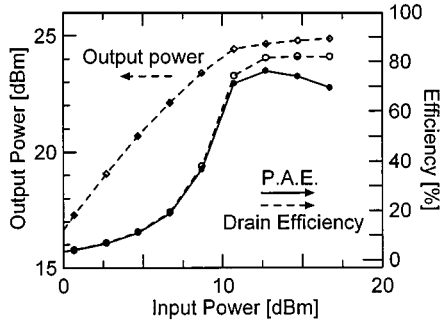


Fig. 8. Measured output power and efficiency ($V_{\rm DD} = 3$ V).

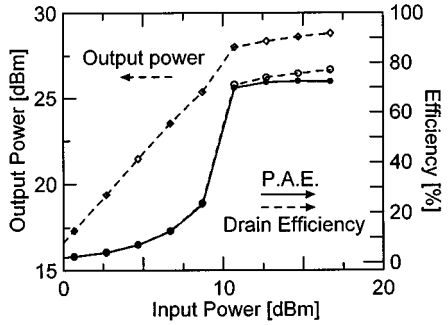


Fig. 9. Measured output power and efficiency ($V_{\rm DD} = 5$ V).

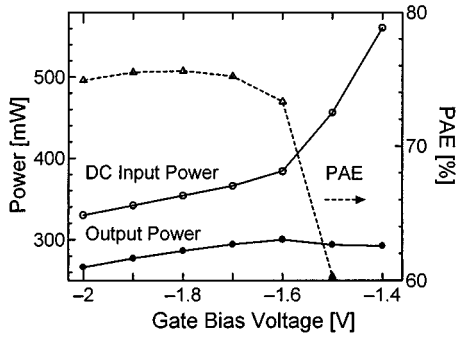


Fig. 10. Output and PAE versus gate bias voltage ($V_{\rm DD} = 3$ V, $P_{\rm IN} = 12.7$ dBm).

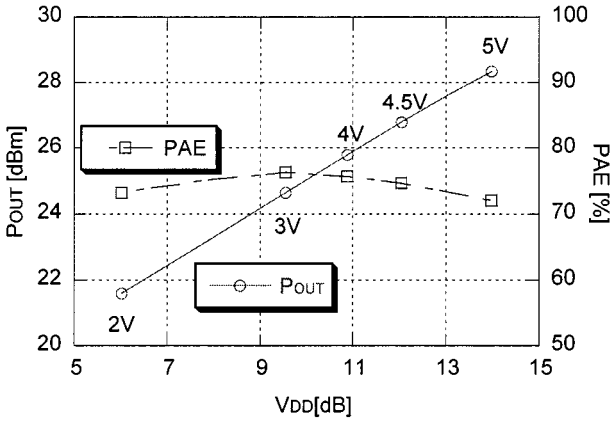
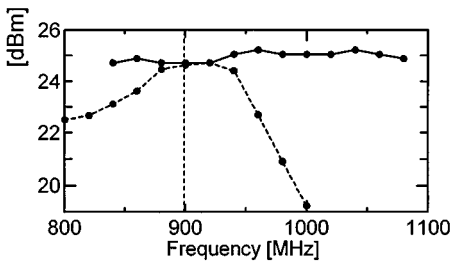
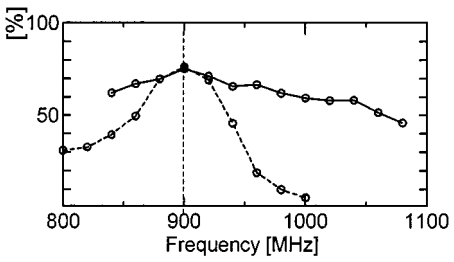


Fig. 11. Output power and efficiency versus VDD ($P_{\rm IN} = 12.7$ dBm).



(a)



(b)

Fig. 12. (a) Output power and (b) PAE versus frequency.

In the regime of low input power (less than 6 dBm for low $V_{\rm DD}$, less than 10 dBm for high $V_{\rm DD}$), the CMCD works as a class-B or class-AB push–pull amplifier (because the parallel filter is an open circuit at the operational frequency). Thus, the structure is an approximately linear amplifier in this regime.

Fig. 10 shows the gate-bias voltage versus dc input power, output power, and PAE at $V_{\rm DD} = 3$ V and $P_{\rm IN} = 12.7$ dBm. PAE stays over 70% when dc bias is below -1.6 V. In the regime of dc bias > -1.6 V, the transistor cannot be in the off state and losses increase rapidly. Fig. 11 shows $V_{\rm DD}$ versus output power and PAE in a decibel scale at $P_{\rm IN} = 12.7$ dBm. $P_{\rm OUT}$ and $V_{\rm DD}$ are linear on a decibel scale, which means $P_{\rm OUT}$ is proportional to the square of $V_{\rm DD}$. At higher $V_{\rm DD}$'s, the output power becomes compressed a little. This is because the transistor power gain is limited and the device does not work well as a switch in this region.

Fig. 12 shows the frequency dependence of output power and PAE. The dotted line shows the CMCD optimized for 900 MHz. The solid line shows the case where the input matching circuits were tuned with variable capacitors at every frequency. This eliminates some of the frequency dependence of the input matching circuits. In this case, the power output becomes almost flat and PAE is greatly improved. This indicates that much of the circuit's bandwidth is a result of input impedance circuits. From the standpoint of harmonic tuning, second harmonics should be presented with an open and third harmonics should be shorted for the CMCD. Balanced circuits are intrinsically open at even harmonics and output capacitances of the transistors and filter tend to be shorted at high frequency. These two are less dependent on the operational frequency and the output load impedance. We believe the CMCD is capable of a large bandwidth when broad-band impedance input matching is used.

VI. System Application

The output of the CMCD amplifier has a nearly constant envelope, dictated by the power supply voltage. Thus, it is appropriate for use with modulated signals of constant envelope. Fig. 13 shows the output spectrum when a global system for mobile communications (GSM) modulated input signal was used

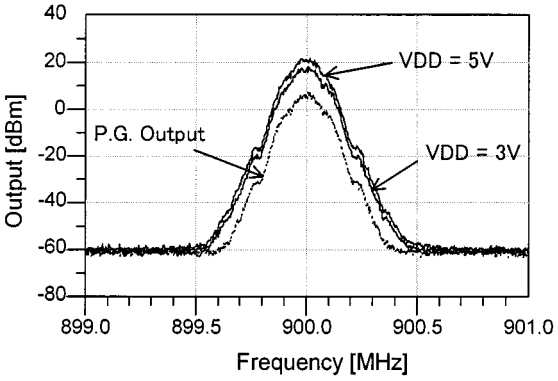


Fig. 13. Output spectrum of the GSM signal.

($P_{\mathrm{IN}} = 12.7$ dBm, $V_{\mathrm{DD}} = 3$ and 5). No major distortion is observed in both cases. The drain efficiency and PAE values were equal to those measured for sinusoidal signals, as shown in Figs. 8 and 9. To apply the CMCD to QPSK or related waveforms with a time-varying envelope, a modulated power supply voltage is required (such as in the Kahn technique).

VII. Conclusion

We have demonstrated for the first time the possibility of current-mode class-D power amplifiers at RF frequencies. Experimental results confirm that high efficiency can be attained and show the possibility of high bandwidth.

References

[1] Krauss, Bostlan, and Rabb, *Solid State Radio Engineering*. New York: Wiley, 1980.

[2] S. El-Hamamsy, "Design of high-efficiency RF class D power amplifier," *IEEE Trans. Power Electron.*, vol. 9, pp. 297–308, May 1994.

[3] N. O. Sokal and A. D. Sokal, "Class E-A new class of high efficiency tuned single-ended power amplifiers," *IEEE J. Solid State Circuits*, vol. SC-10, pp. 168–176, June 1975.

[4] J. Staudinger, "Multiharmonic load termination effects on GaAs MESFET power amplifiers," *Microwave J.*, pp. 60–77, Apr. 1996.

[5] C. Duvanaud, S. Dietsche, G. Pataut, and J. Obregon, "High-efficient class F GaAs FET amplifier operating with very low bias voltages for use in mobile telephones at 1.75 GHz," *IEEE Microwave Guided Wave Lett.*, vol. 3, pp. 268–270, Aug. 1993.

[6] A. Inoue, T. Heima, A. Ohta, R. Hattori, and Y. Mitsui, "Analysis of class-F and inverse class-F amplifiers," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, 2000, pp. 775–778.

[7] C. J. Wei, P. DiCarlo, Y. A. Tkachenko, R. McMorrow, and D. Bartle, "Analysis and experimental waveform study on inverse class-F mode of microwave power FETs," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, 2000, pp. 525–528.

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